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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,125	04/15/2004	Cheng-Yuan Hsu	11808-US-PA	3124

31561 7590 09/27/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,125	HSU ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1-12 are objected to because of the following informalities and/or defects:

Claims 1 and 7 each need to clarify how many erased gates are between each pair of neighboring gate structures; and, how many dielectric layers are in each gate structure.

Claims 1 and 7 each need to clarify what are the relationship between the recited gate structures and the recited outmost gate structures.

Claims 6 and 12 each need to clarify which of the different types of dielectric layers the term of "the dielectric layer" definitely refers to.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (Chen et al., US 20040057286).

Chen discloses a NAND flash memory cell row (Figs. 2, 5, 6 and 8; also see [0031], and [0037]-[0046]), comprising: a substrate (52); a plurality of gate structures, each of the gate structures comprising: a tunneling dielectric layer (40), a floating gate (37; polysilicon layer doped with arsenic), an inter-gate dielectric layer (42; ONO) and a control gate (36); a plurality of doped regions (49), disposed in the substrate between the gate structures, wherein the gate structures are connected in series; a plurality of erase gates (43), disposed over the doped regions and between the gate structures; a plurality of spacers (47), disposed between the gate structures and the erase gates; a plurality of dielectric layers (53), disposed between the erase gates and the doped regions; first and second select gates (44 and 45), disposed on each of the sidewalls of two outermost gate structures respectively; a plurality of select gate dielectric layers (54; abut 100 Angstroms, see [0046]), disposed between the first select gate and the substrate and between the second select gate and the substrate; a drain region (50), disposed in the substrate, wherein the drain region is disposed on one side of the first select gate corresponding to the gate structures; and a source region (51), disposed in the substrate, wherein the source region is disposed on one side of the second select gate corresponding to the gate structures; a plurality of word lines (CG), arranged in parallel along column direction, and each of the word lines is coupled to the control gates of the gate structures in a column; a plurality of bit lines (BL), arranged in parallel

along row direction, each of the bit lines is coupled to the drain region of the first select gate in a row; a source line (CS), coupled to the source regions of the second select gates in the same column respectively; and a plurality of erase gate lines (EG), arranged in parallel along column direction, and coupled to the erase gates in the same column.

Regarding claims 6 and 12, the dielectric layer (53) between the erase gate electrode and the doped region in Chen can have thickness that is comparable with that of the select gate dielectric layer (54), which can be about 300-400 Angstroms, as shown in Fig. 2, and also see [0034] and/or [0046]).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-E are cited as being related to a flash memory cell structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
September 21, 2005

SHOUXIANG HU
PRIMARY EXAMINER